REMARKS

A total of 17 claims remain in the present application. The foregoing amendments are presented in response to the Office Action mailed August 7, 2007, wherefore reconsideration of this application is requested.

By way of the above-noted amendments, claims 18-20 have been cancelled. Clearly, no new subject matter has been introduced.

Referring now to the text of the Office Action:

- claims 18 and 20 stand objected to under 35 U.S.C. § 101 as being directed to non-statutory Subject Matter;

- claims 1, 11-15 and 17-20 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of United States Patent Application Publication No. 2003/0084409 (Abt et al.) in view of United States Patent No. 5,038,285 (Jouandet);

- claims 2-6, 9 and 10 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of Abt et al. in view of Jouandet, and further in view of United States Patent No. 6,330,354 (Companion et al.) in view of United States Patent No. 5,272,763 (Maruyama);

- claims 7 and 8 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of Abt et al., Jouandet, Companion et al., and Maruyama, and further in view of "Robotics, "Image Processing Techniques for Machine Vision" (Martin et al.); and

- claim 16 stands rejected under 35 U.S.C. § 103(a), as being unpatentable over the teaching of Abt et al. in view of Jouandet, and further in view of United States Patent No. 6,808,591 (Phan et al.).

The Examiners above-noted claim rejections are believed to be traversed by the above-noted claim amendments, and further in view of the following discussion.

Rejections under 35 U.S.C. § 101

The rejections of claims 18 and 20 under 35 U.S.C. § 101 are traversed by way of the above-noted cancellation of these claims.

Rejections under 35 U.S.C. § 103

As best understood by the Applicant, the Examiner's rejections under 35 U.S.C. § 103 are based the premise that that Abt et al. broadly teaches the intent of the claimed invention (i.e. deriving a 3-D model of a semiconductor chip based on mosaic images), but none of the detailed steps set out in claim 1. The Examiner then appears to find each of the "missing" steps in the Jouandet patent, and argues that it would be obvious to modify the teaching of Abt et al to perform the various steps "as suggested by Jouandet, to 'produce two-dimensional maps of three-dimensional surfaces' that 'reduc[es] distortion between the straight lines representations'. Applicant respectfully disagrees with both the Examiner's analysis and his conclusions with respect to patentability of claims 1-20.

United States Patent Application Publication No. 2003/0084409 (Abt et al.) broadly teaches a method and system for extracting circuit information from images of an integrated circuit (IC). As may be seen in FIG. 1 and as described at paragraphs 42-44 , Abt et al. teaches that images of each layer of the IC are processed to create a vector representation, which are then aligned vertically and horizontally, and the aligned images used to generate schematics of the circuit [see step 17]. The person of ordinary skill in the art will recognise that a "schematics of the circuit" are a 2-dimensional representation of the IC circuit, using conventional symbolic representations of electronic components (such as transistors, logic gates etc., as shown in FIGs. 12 and 13). As such, the person of ordinary skill in the art will recognise that Abt et al does not attempt to teach a method of producing a three-dimensional model of a semiconductor chip, as defined in claim 1. In that respect, the person of ordinary skill in the art will recognise that the difference between a 2-dimentional circuit schematic and a 3-dimensional model is both glaring and unmistakable.

The Examiner has admitted that Abt et a. fails to teach any of the detailed steps as set out in claim 1. As discussed above, it will be seen the Abt et al. also fail to teach or suggest the problem to be solved by the present invention. Nor do Abt et al. teach a method or system that yields the results obtained by the present invention; that is, a three-dimensional model of the IC. Thus it will be seen that Abt et al is entirely unrelated to the presently claimed invention. Jouandet fails to provide the missing teaching.

United States Patent No. 5,038,285 (Jouandet) teaches a method "for deriving a planar representation of a three-dimensional surface." [Abstract], based on computer tomography image slices. More particularly, Jouandet teaches a method and system of deriving a 2-dimentional map of the surface of a human brain, by analysing multiple computer tomography image slices.

"To rely on a reference under 35 U.S.C. § 103, it must be analogous prior art" [MPEP 2141.01(a)(I)] Applicant respectfully submits that Jouandet is clearly not analogous prior art, and so cannot properly be relied upon to support rejections under 35 U.S.C. § 103. More particularly:

- Jouandet teaches a method "for deriving a planar representation of a three-dimensional surface." The present invention does not attempt to do this.

- Present claim 1 defines "a method for producing a three-dimensional model of a semiconductor chip" Jouandet does not attempt do this, and it is not at all clear if it would even be possible to obtain a three-dimensional model of an IC chip using the methods of Jouandet. In that respect, it will be noted that computer tomography image slices are images of a structure (in this case, the human brain) viewed in cross section, so that the contours being viewed are cross-sections of continuous surfaces that extend through many successive slices (images). Implicit in the methodology of Jouandet is that the spacing between the slices is small enough that the image in one slice is a recognizable variation of the image of an adjacent slice. In contrast, the mosaic images of the present invention (and Abt et

al.) are images of respective layers of the IC chip. The IC structures being viewed are, with the exception of vias, completely discontinuous between layers (and thus images), and in all non-trivial cases the image of one layer will look nothing like that of the adjacent layer. In this situation, it is not at all clear how the method of Jouandet could be used to obtain a useful result, much less a three-dimensional model of the IC chip.

- Jouandet teaches that the solution of the '285 patent solves the problem of distortions in the 2-dimensional map due to the straight-line representations of the contours in each CT image. No such problem exists in the context of the present invention, for at least the reason that the contours of an IC chip are (or can be accurately represented by) straight lines.

- The present invention solves the problem of how to achieve accurate vertical alignment between discontinuous structures in coarsely aligned mosaic images. Abt et al vaguely mentions that this step is performed (FIG. 1 at reference 14) but provides no teaching of how it is done. Jouandet simply does not address this issue at all, and it is not clear how the teaching of Jouandet might be modified (or used to modify Abt et al.) to solve this problem.

In light of the foregoing, it is respectfully submitted that United States Patent No. 5,038,285 (Jouandet) is non-analogous prior art, and cannot properly be relied upon to support a rejection under 35 U.S.C. § 103. If, however, the Examiner is un-persuaded by the above arguments, it will also be noted that Jouandet fails to teach or fairly suggest the features of the presently claimed invention. More particularly, and with specific reference to claim 1, Jouandet fails to teach or fairly suggest "establishing virtual reference marks using end points of different mosaic images that are vertically aligned to within an uncertainty of the coarse alignment of the mosaic images; using the virtual reference marks to adjust x and y coordinates of each of the mosaic images to derive a three dimensional coordinate space; and processing the end points within the three dimensional coordinate space to define vias, lines and branch lines of the semiconductor chip, interconnected to define the three-dimensional model."

According to Jouandet, reference points are defined at the "intersections between the crestlines and the sulci along brain slice surface" [Col 5, lines 40-43] The crestlines are computer generated concentric lines [Col 5, lines 28-38], while the "sulci along brain slice surface" are detected in the brain slice image. The person of ordinary skill in the art will appreciate that the resulting reference points serve the purpose of sampling the contour of the sulci in the brain image slice at reasonably spaced intervals. However, the person of ordinary skill in the art will equally recognise that Jouandet's reference points do not relate to endpoints of anything, much less endpoints in different mosaic images Furthermore, Jouandet does not teach or suggest that these reference points are used to adjust x and y coordinates of each of the mosaic images to derive a three dimensional coordinate space; and does not teach or suggest subsequently "processing the endpoints within the three-dimensional coordinate space to define vias, lines and branch lines of the semiconductor chip, interconnected to define the three-dimensional model" , all as required by claim 1.

Thus it will be seen that Jouandet is both non-analogous prior art, and fails to teach or fairly suggest features of the present invention.

In light of the foregoing, it is respectfully submitted that the presently claimed invention is clearly distinguishable over the teaching of the cited references, taken alone or in any combination. Thus it is believed that the present application is in condition for allowance, and early action in that respect is courteously solicited.

Respectfully submitted,

/Kent Daniels/

Kent Daniels, P.Eng.
Registration No. 44,206
Customer No. 020988

1981 McGill College Avenue
Suite 1600
Montreal, QC H3A 2Y3
Canada